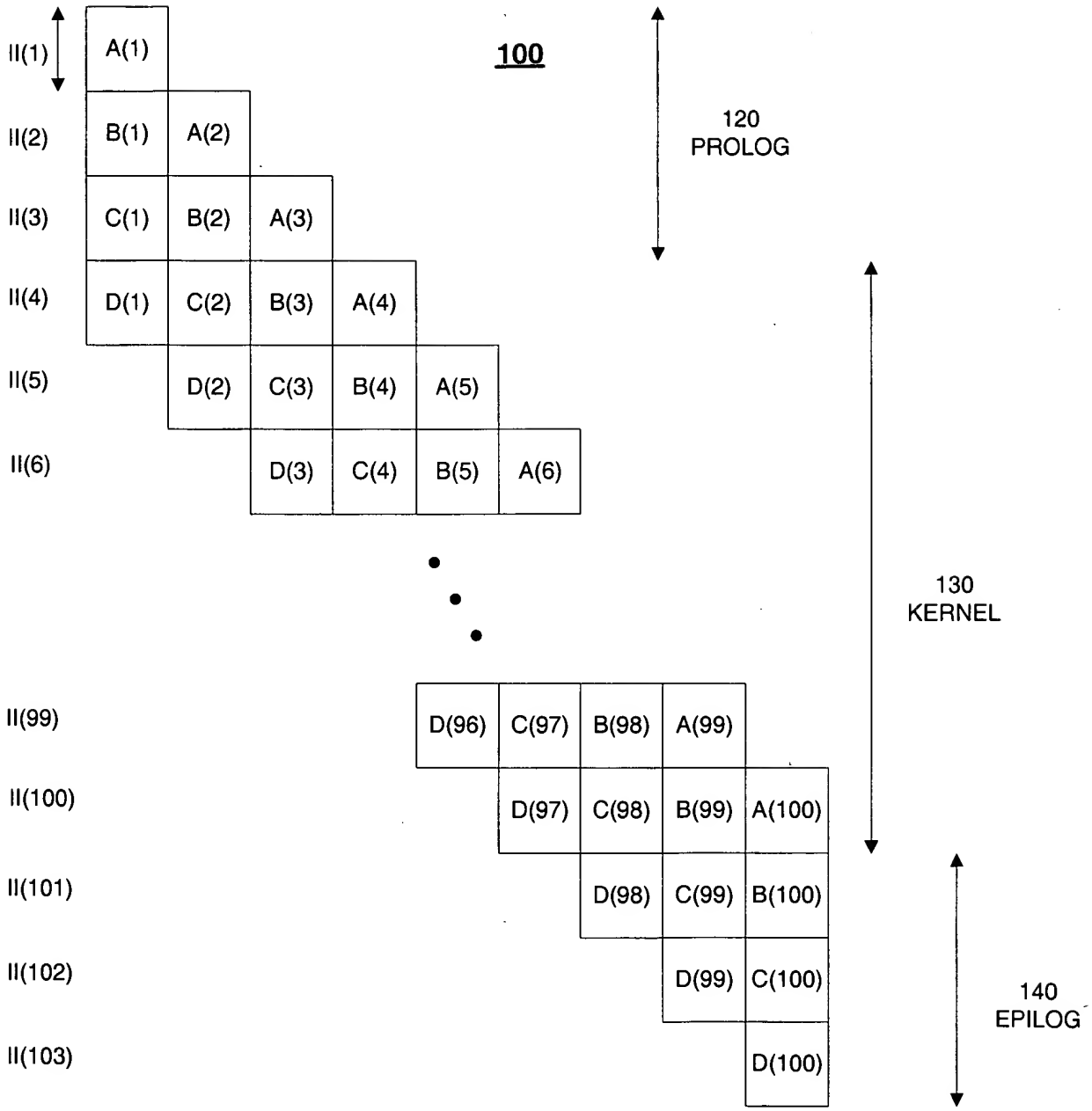

100
II(1)
A(1)
II(2)
B(1)
A(2)
II(3)
C(1)
B(2)
A(3)
II(4)
D(1)
C(2)
B(3)
A(4)
II(5)
D(2)
C(3)
B(4)
A(5)
II(6)
D(3)
C(4)
B(5)
A(6)
120
PROLOG
130
KERNEL
II(99)
D(96)
C(97)
B(98)
A(99)
II(100)
D(97)
C(98)
B(99)
A(100)
II(101)
D(98)
C(99)
B(100)
II(102)
D(99)
C(100)
II(103)
D(100)
140
EPILOG

Fig. 1A

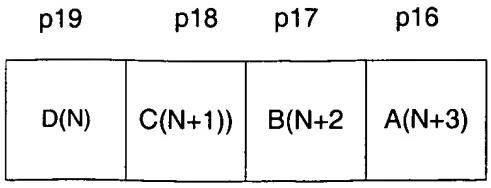
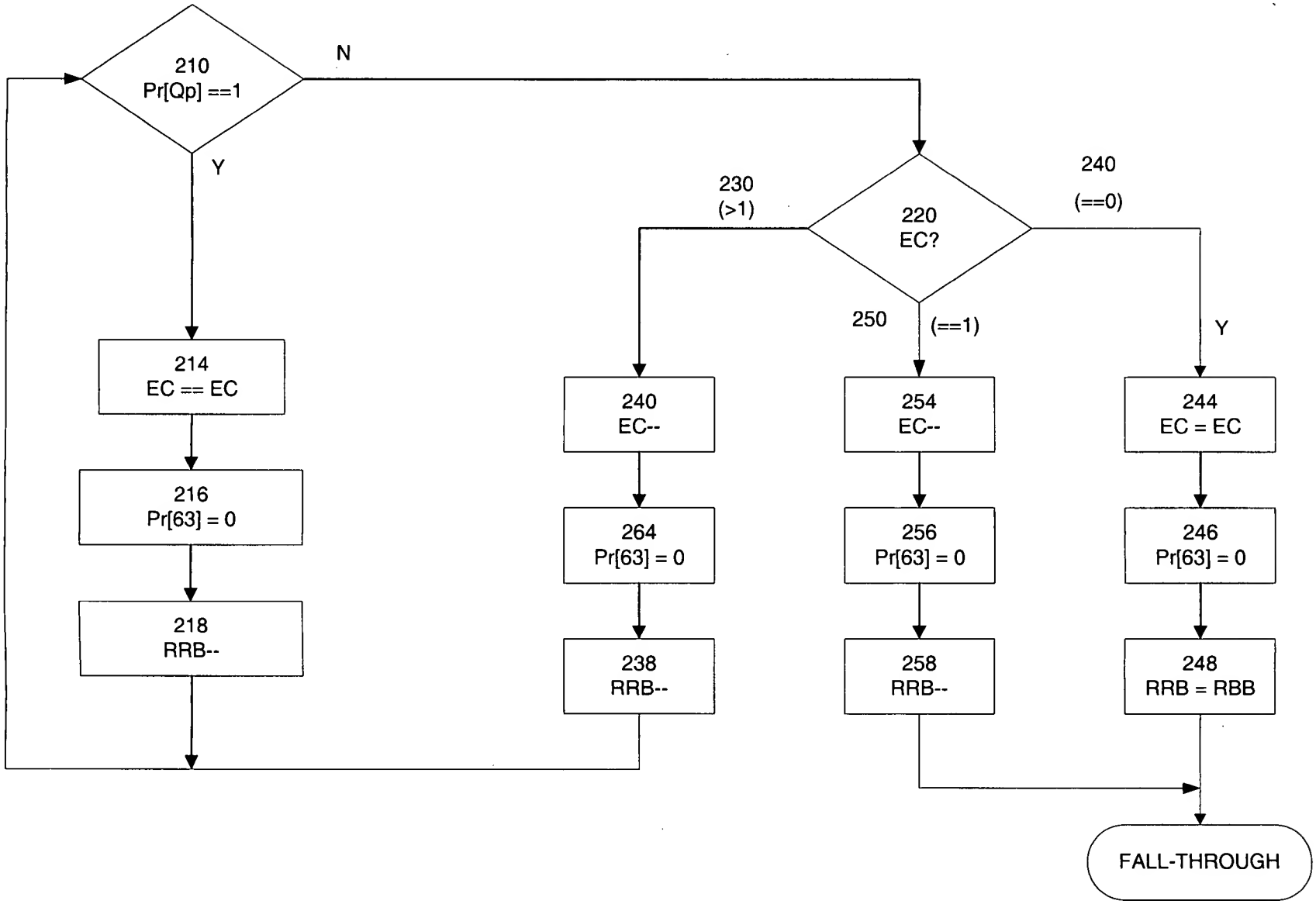

p19
p18
p17
p16
D(N)
C(N+1))
B(N+2
A(N+3)

Fig. 1B

Fig. 2

200


210
Pr[Qp] ==1
N
Y
220
EC?
230
(>1)
240
(==0)
250
(==1)
Y
214
EC == EC
216
Pr[63] = 0
218
RRB--
240
EC--
264
Pr[63] = 0
238
RRB--
254
EC--
256
Pr[63] = 0
258
RRB--
244
EC = EC
246
Pr[63] = 0
248
RRB = RBB
FALL-THROUGH

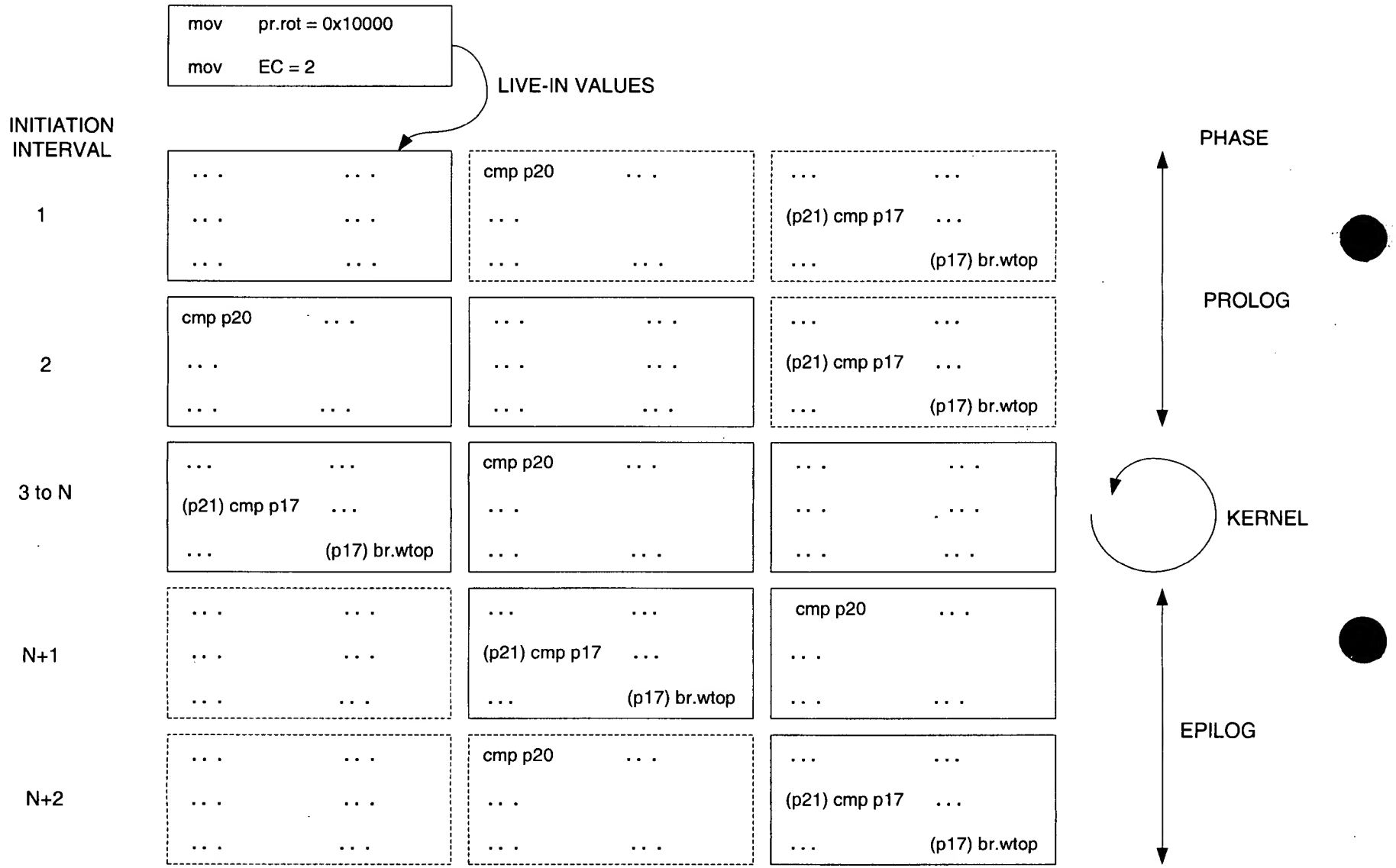

mov pr.rot = 0x10000
mov EC = 2
LIVE-IN VALUES
INITIATION INTERVAL
1
2
3 to N
N+1
N+2
cmp p20
(p21) cmp p17
(p17) br.wtop
PHASE
PROLOG
KERNEL
EPILOG

Fig. 3A

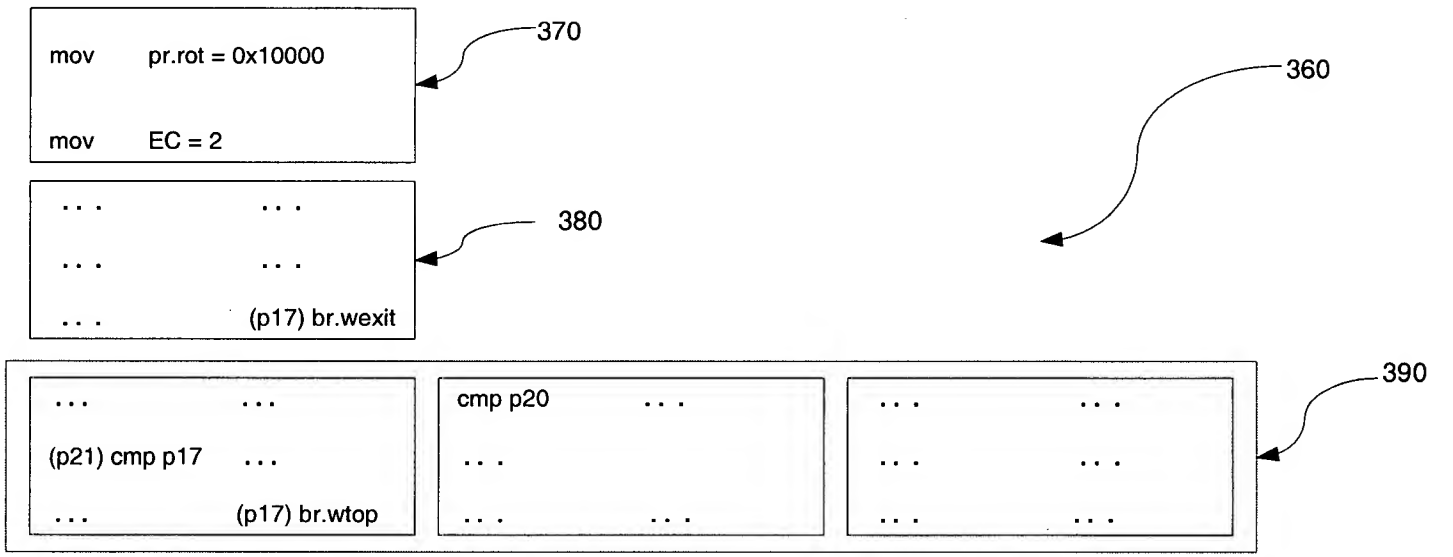

mov pr.rot = 0x10000
mov EC = 2
370
360
380
(p17) br.wexit
390
(p21) cmp p17
(p17) br.wtop
cmp p20

Fig. 3B

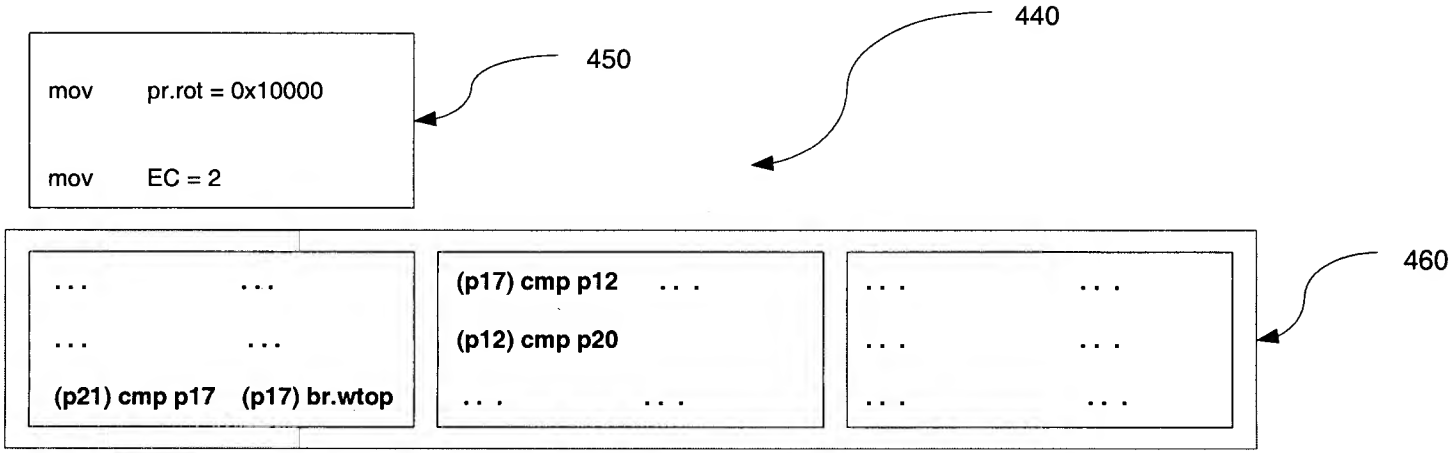

mov pr.rot = 0x10000
mov EC = 2
450
440
460
(p21) cmp p17
(p17) br.wtop
(p17) cmp p12
(p12) cmp p20

Fig. 4B

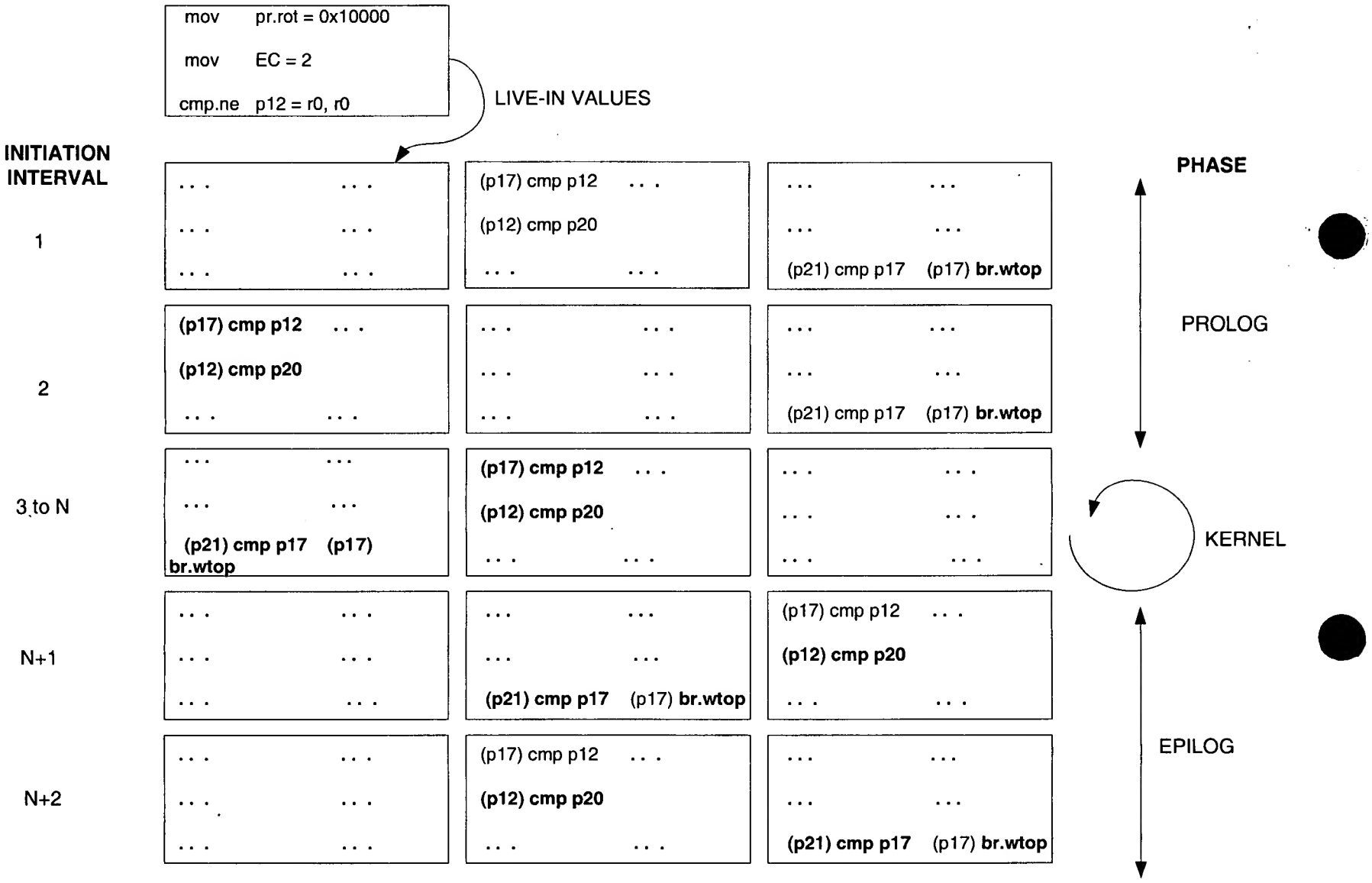

mov pr.rot = 0x10000
mov EC = 2
cmp.ne p12 = r0, r0
LIVE-IN VALUES
INITIATION INTERVAL
PHASE
1
2
3 to N
N+1
N+2
(p17) cmp p12
(p12) cmp p20
(p21) cmp p17 (p17) br.wtop
PROLOG
KERNEL
EPILOG

Fig. 4A

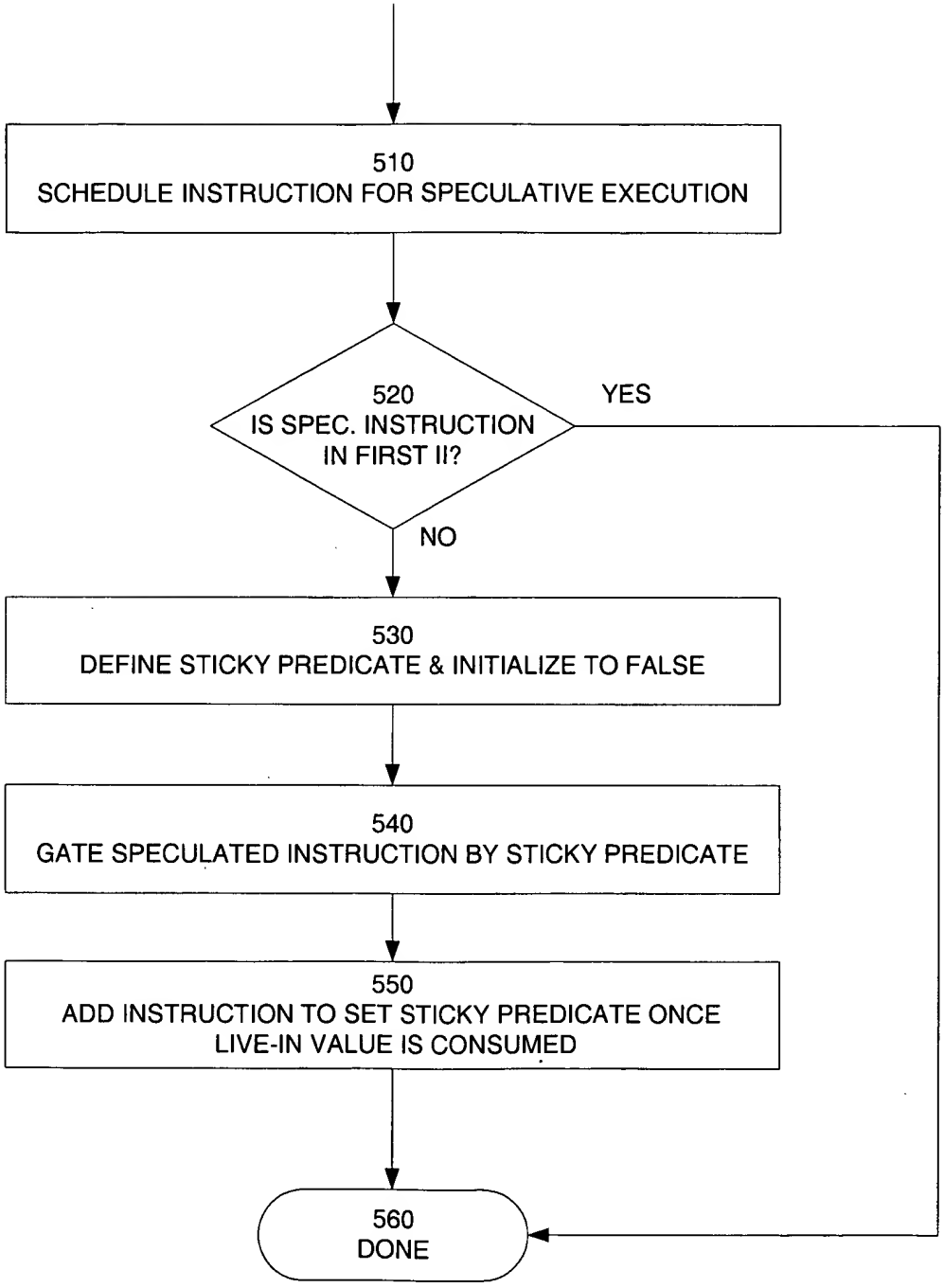

510
SCHEDULE INSTRUCTION FOR SPECULATIVE EXECUTION
520
IS SPEC. INSTRUCTION IN FIRST II?
YES
NO
530
DEFINE STICKY PREDICATE & INITIALIZE TO FALSE
540
GATE SPECULATED INSTRUCTION BY STICKY PREDICATE
550
ADD INSTRUCTION TO SET STICKY PREDICATE ONCE LIVE-IN VALUE IS CONSUMED
560
DONE

Fig. 5

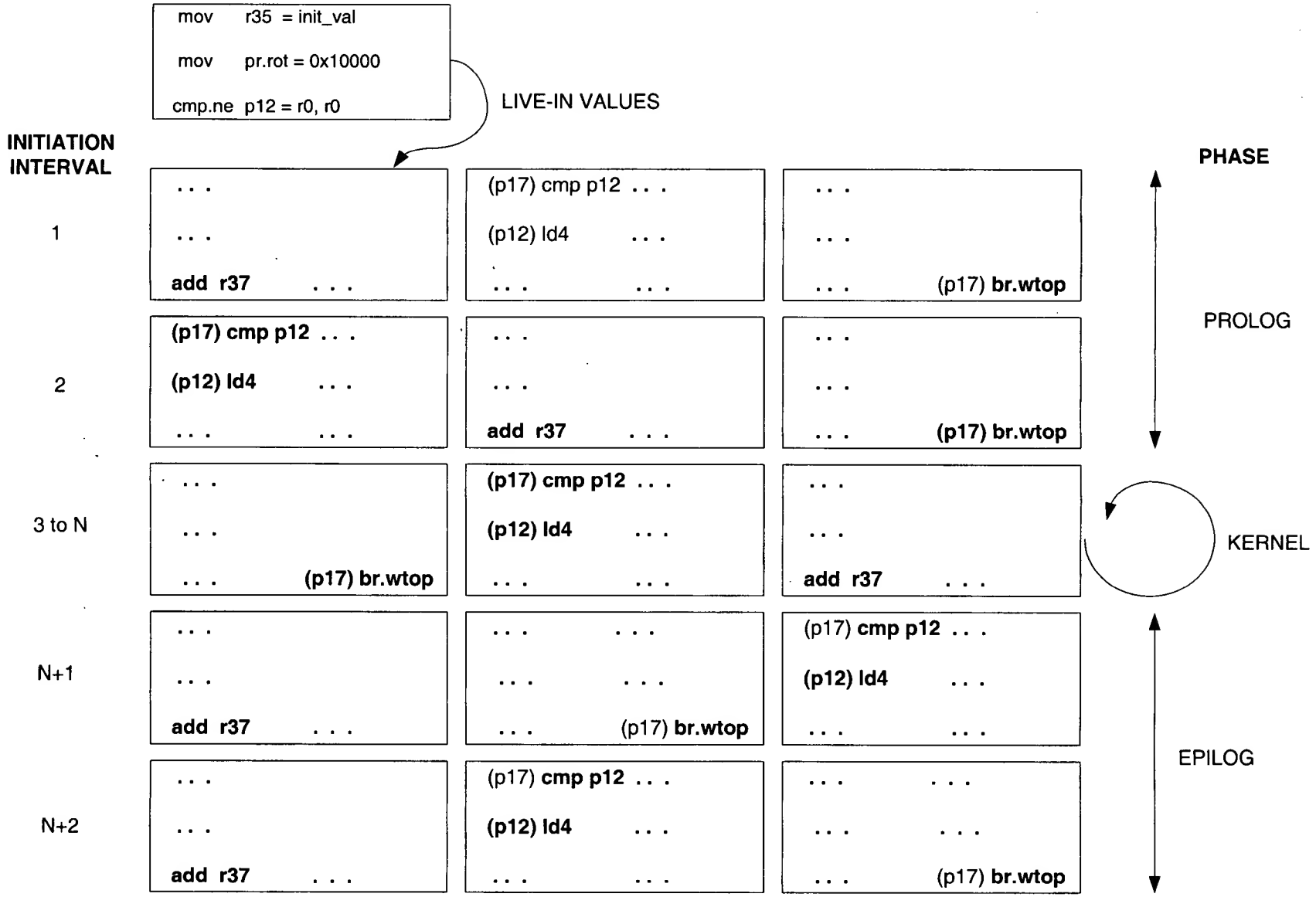

mov r35 = init_val
mov pr.rot = 0x10000
cmp.ne p12 = r0, r0
LIVE-IN VALUES
INITIATION INTERVAL
PHASE
1
2
3 to N
N+1
N+2
add r37
(p17) cmp p12
(p12) ld4
(p17) br.wtop
PROLOG
KERNEL
EPILOG

Fig. 6

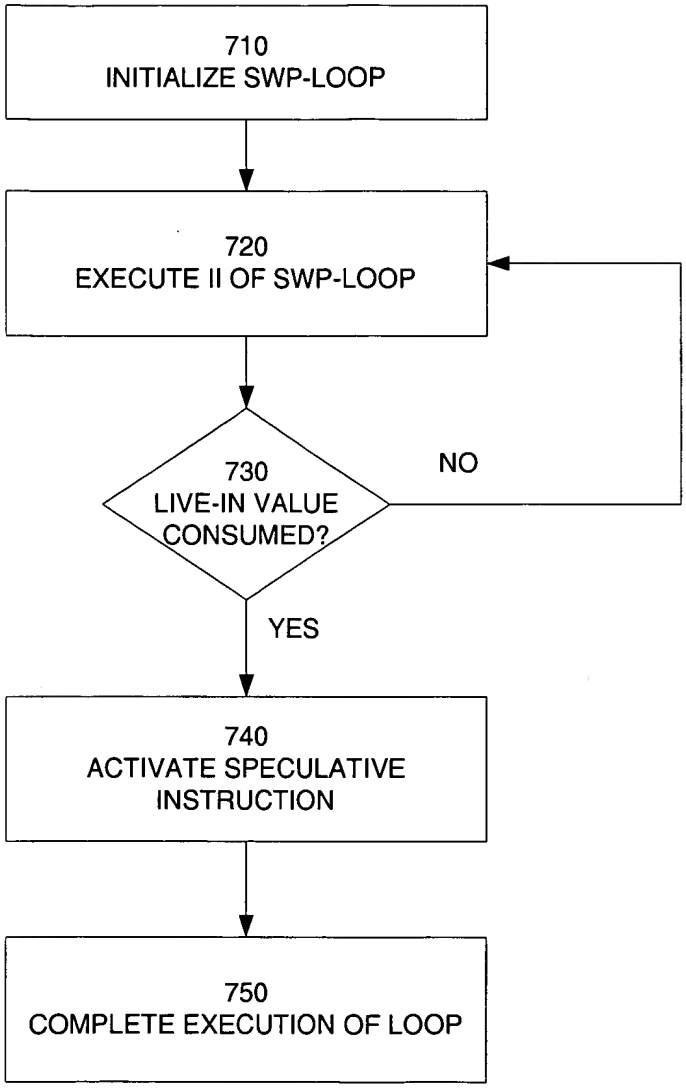

710
INITIALIZE SWP-LOOP
720
EXECUTE II OF SWP-LOOP
730
LIVE-IN VALUE
CONSUMED?
NO
YES
740
ACTIVATE SPECULATIVE
INSTRUCTION
750
COMPLETE EXECUTION OF LOOP

Fig. 7

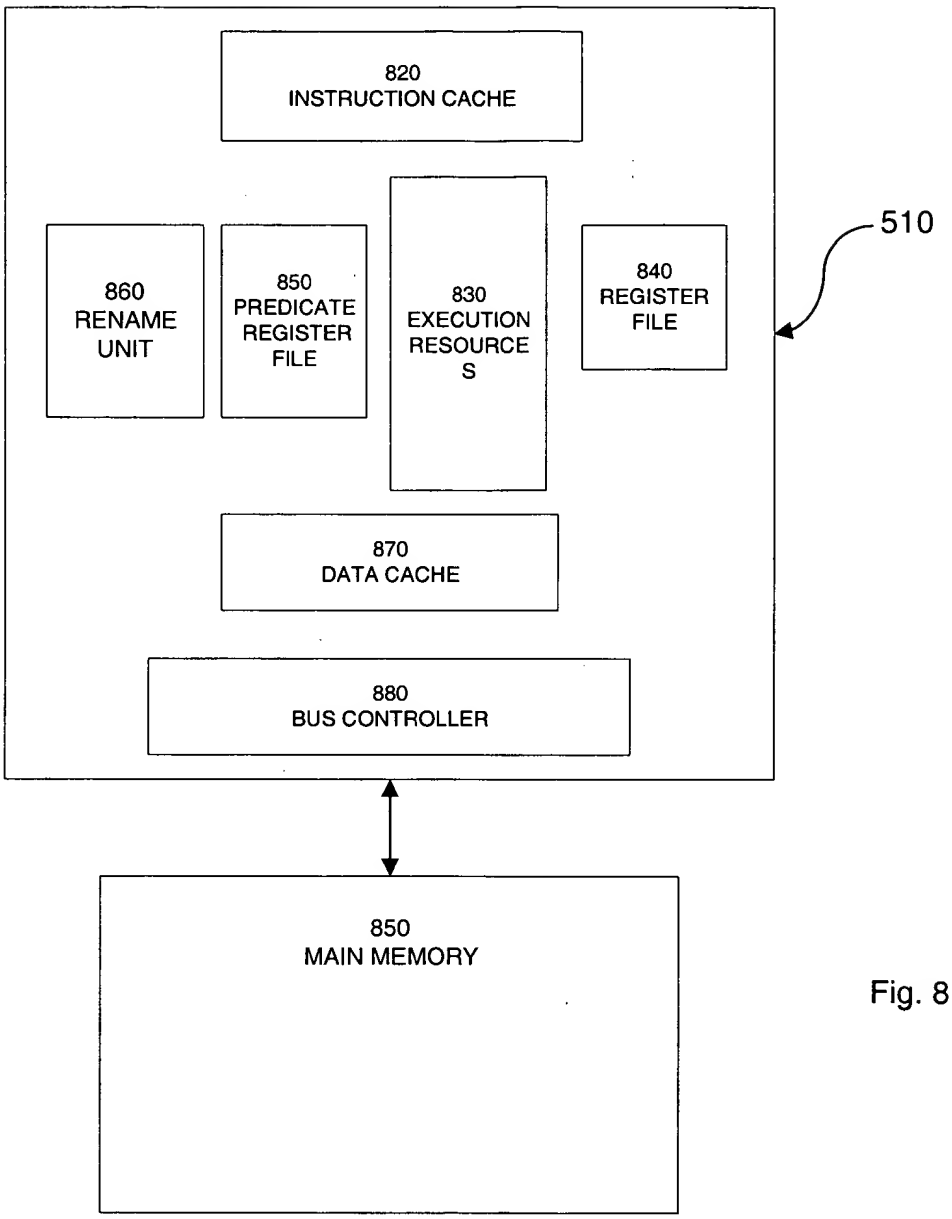

800
820
INSTRUCTION CACHE
860
RENAME
UNIT
850
PREDICATE
REGISTER
FILE
830
EXECUTION
RESOURCE
S
840
REGISTER
FILE
510
870
DATA CACHE
880
BUS CONTROLLER
850
MAIN MEMORY

Fig. 8